

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-14 have been canceled.

Claim 15 (Currently Amended): A bit stream processor, comprising:

a memory having one or more inputs for receiving respective input bit streams, said input bit streams of said one or more inputs defining a plurality sequence of input combinations to said memory;

5 an opcode input of said memory for inputting a selected ~~one of one or more opcodes~~ opcode, which said selected ~~one of said one or more opcodes~~ is associated with a function wherein said associated function operates on said sequence of input combinations to generate an output bit stream; and

an output of said memory for outputting an output bit stream.

Claim 16 (Currently Amended): The processor of Claim 15, wherein said memory is a bit-addressable memory where each said input combination of said plurality sequence of input combinations is mapped to a unique bit location in said memory.

Claim 17 (Original): The processor of Claim 15, wherein said memory comprises binary memory devices which can be individually and selectively read.

Claim 18 (Currently Amended): The processor of Claim 15, wherein said sequence of input combinations comprise separate address inputs which are selected by said ~~select one of said one or more opcodes~~ associated function.

Claim 19 (Currently Amended): The processor of Claim 15, wherein ~~the processor generates said output bit stream at said output as a~~ said associated function is a function of one or more Boolean operations performed on said input bit streams.

AMENDMENT AND RESPONSE

S/N 09/389,567

Atty. Dkt. No. OGPT-24,727

3

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Claim 20 (Currently Amended): The processor of Claim 15, wherein each said input combination of said ~~plurality~~ sequence of input combinations at said one or more inputs is operated on by said ~~opcode~~ associated function.

Claim 21 (Original): The processor of Claim 15, wherein each of said one or more inputs accommodates a single serial bit stream.

Claim 22 (Currently Amended): The processor of Claim 15, wherein said opcode is associated with a function defined by a predetermined set of Boolean operations.

Claim 23 (Currently Amended): The processor of Claim 16, wherein said ~~opcode~~ function is generated represented by a ~~from a~~ lookup table having mapping a finite number of said input combinations mapped to a respective single bit results, said respective single bit results obtained in accordance with the by applying a set of predetermined Boolean operations to said input combinations.

Claim 24 (Currently Amended): The processor of Claim 23, wherein each said respective single bit results of said finite number of said input combinations is used to generate a string of said single bit results which define said ~~opcode~~ associated function.

Claim 25 (Currently Amended): A method for bit stream processing, comprising the steps of:

5 providing a memory having one or more inputs for receiving respective input bit streams, the input bit streams of the one or more inputs defining a ~~plurality~~ sequence of input combinations to the memory;

inputting a selected ~~one of one or more opcodes~~ opcode at an opcode input of the memory, which the selected ~~one of the one or more opcodes~~ opcode is associated with a function wherein said associated function operates on the input combinations to generate an output bit stream; and

10 outputting an output bit stream at an output of the memory.

AMENDMENT AND RESPONSE

S/N 09/389,567

Atty. Dkt. No. OGPT-24,727

C1 Claim 26 (Currently Amended): The method of Claim 25, wherein the memory in the step of providing is a bit-addressable memory where each input combination of the plurality sequence of input combinations is mapped to a unique bit location in the memory.

Claim 27 (Original): The method of Claim 25, wherein the memory in the step of providing comprises binary memory devices which can be individually and selectively read.

Claim 28 (Currently Amended): The method of Claim 25, wherein the plurality sequence of input combinations in the step of providing comprise separate address inputs which are selected by the ~~select one of the one or more opcodes~~ associated function.

Claim 29 (Currently Amended): The method of Claim 25, wherein the processor associated function in the step of ~~outputting~~ generates the output bit stream at the output as outputting is a function of one or more Boolean operations performed on the input bit streams.

Claim 30 (Currently Amended): The method of Claim 25, wherein each input combination of the plurality sequence of input combinations at the one or more inputs is operated on individually by the opcode associated function, in the step of inputting.

Claim 31 (Original): The method of Claim 25, wherein each of the one or more inputs in the step of providing accommodates a single serial bit stream.

Claim 32 (Currently Amended): The method of Claim 25, wherein the opcode in the step of inputting is associated with a function defined by a predetermined set of Boolean operations.

AMENDMENT AND RESPONSE
S/N 09/389,567
Atty. Dkt. No. OGPT-24,727

5

C/ Claim 33 (Currently Amended): The method of Claim 26, wherein the opcode associated function is generated represented by a from a lookup table having mapping a finite number of the input combinations mapped to [[a]] respective single bit result results, the single bit results obtained in accordance with the by applying a set of predetermined Boolean operations to said input combinations.

Claim 34 (Currently Amended): The method of Claim 33, wherein each the respective single bit results of the finite number of the input combinations is used to generate a string of the single bit results which define the opcode associated function.

AMENDMENT AND RESPONSE

S/N 09/389,567

Atty. Dkt. No. OGPT-24,727